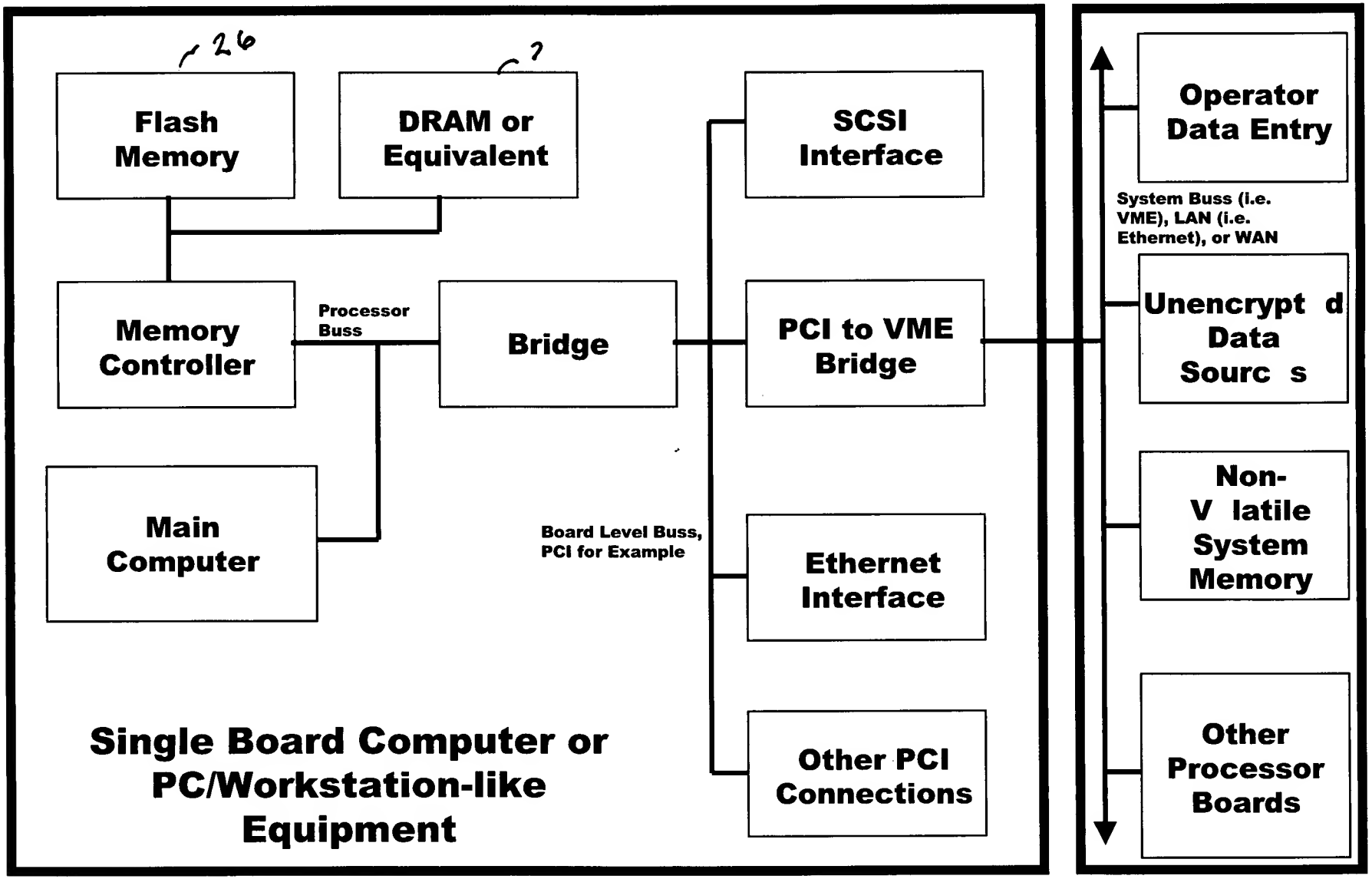

Fig. 1 Prior Art Processor Board Connected to Typical Sy t m El m nts

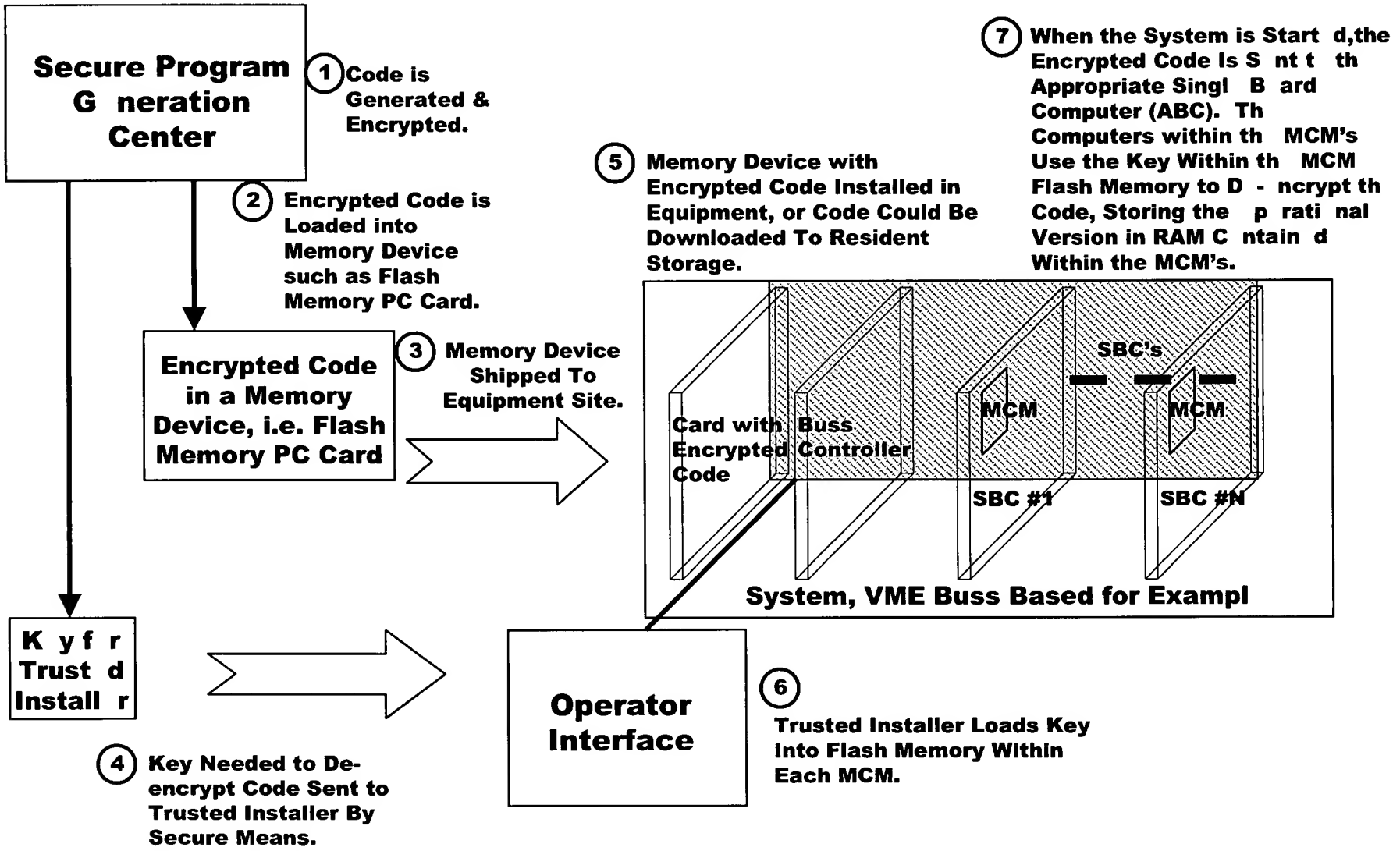

Fig. 2 Architecture For A Tamperproof Computer System

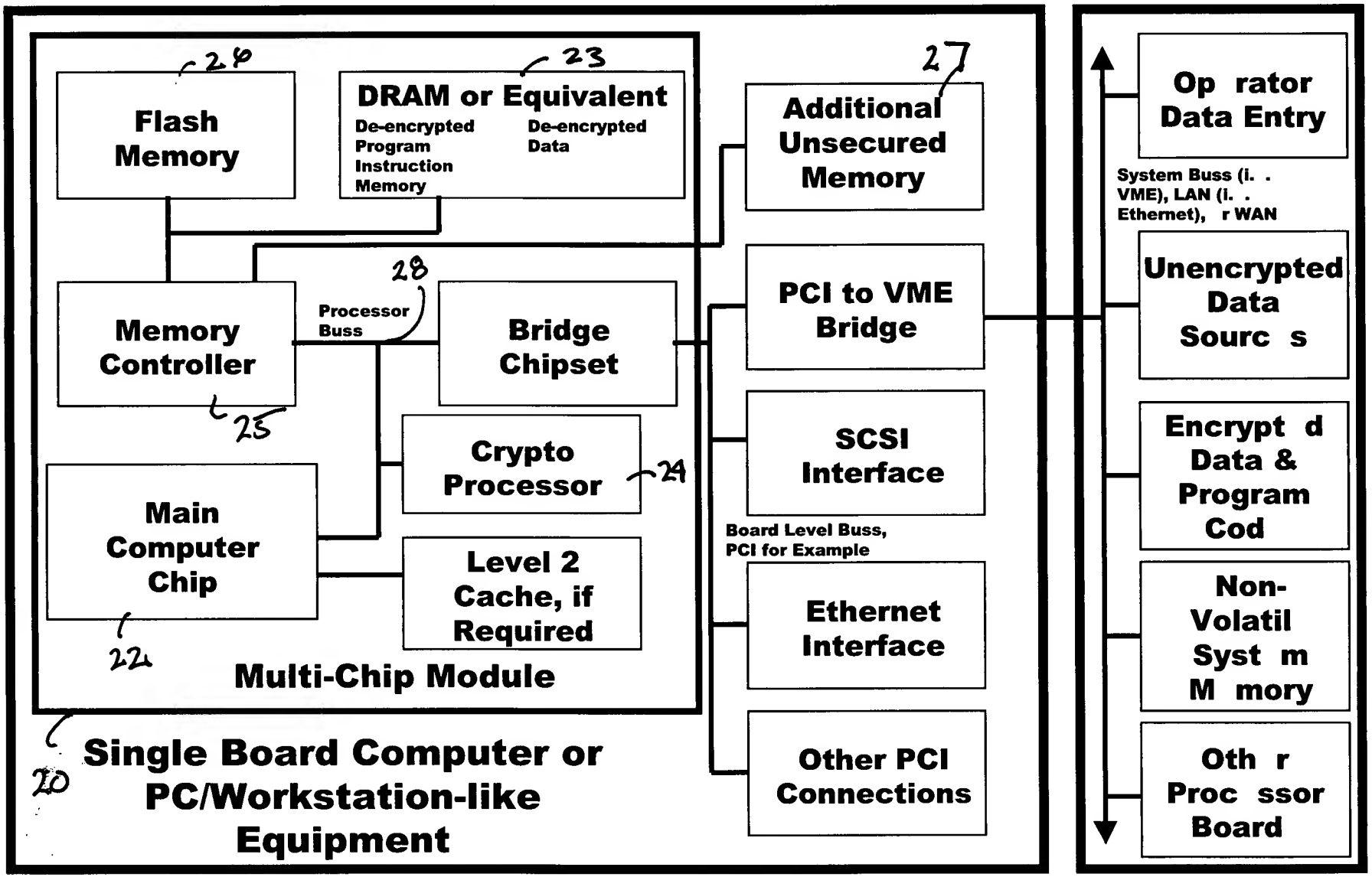

Fig. 3 Processor Board With De-Encryption Within A Multi-Chip Modul

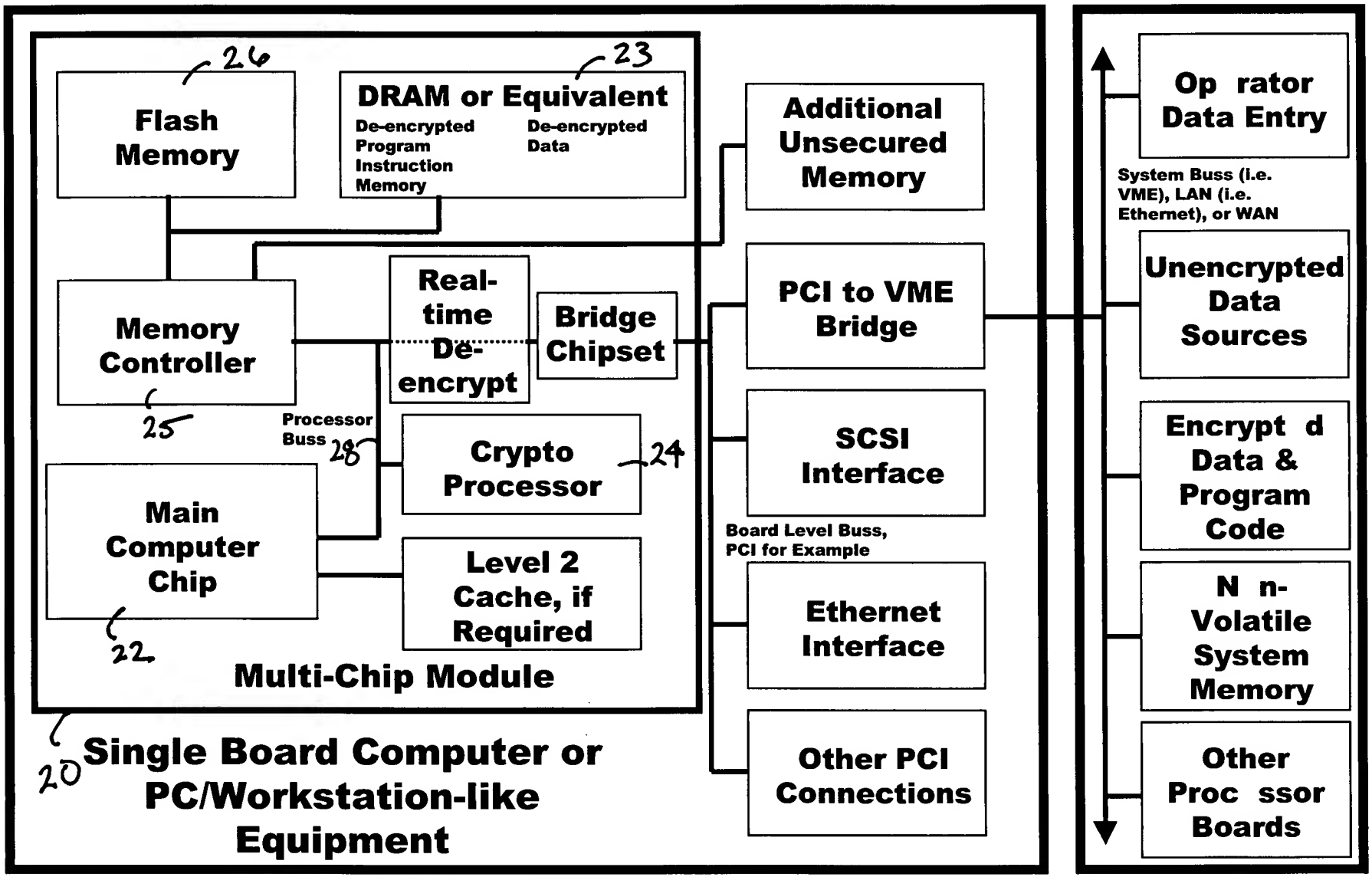

Fig. 4 Processor Board With Multiple De-Encryption D vice Within A Multi-Chip Modul

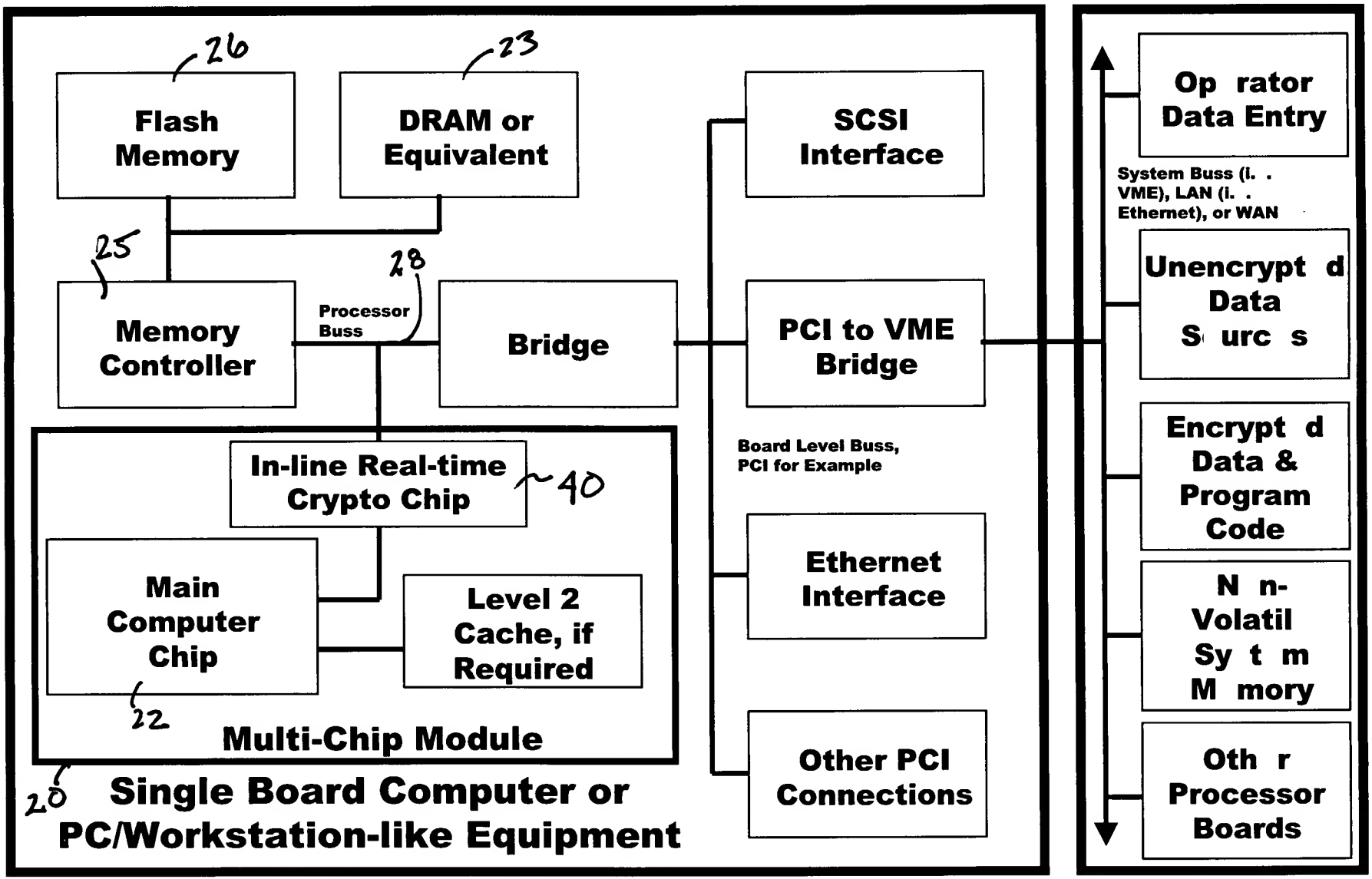

Fig. 5 Processor Board With In-line Real-time De-Encryption Within A Multi-Chip Modul